

What is claimed is:

- 1 1. A method for simulating hardware circuits during which voltages are  
2 calculated at a plurality of circuit nodes, comprising the steps of:  
3 (a) carrying out a first DC-simulation run at the begin of a functional  
4 cycle,  
5 (b) carrying out a second DC-simulation run at the end of said cycle,  
6 (c) comparing simulated values from both runs at respective circuit  
7 nodes, and  
8 (d) storing mismatch information about static error afflicted nodes at  
9 which the calculated values differ by more than a predetermined  
10 first threshold value.
- 1 2. The method according to claim 1 further comprising the steps of:  
2 (e) putting out said mismatch information for a manual correction,  
3 (f) carrying out a transient analysis covering the same functional cycle  
4 after correction,  
5 (g) comparing calculated values from said analysis with calculated  
6 values from said first or second DC simulation run at respective  
7 circuit nodes, and  
8 (h) storing mismatch information about dynamic error afflicted nodes at  
9 which the calculated values differ by more than a predetermined  
10 second threshold value.
- 1 3. The method according to claim 2 further comprising the step of  
2 automatically correcting dynamic errors in a simulation input file.
- 1 4. The method according to 3 claim further comprising the step of performing  
2 an iterative hardware simulation with the corrected simulation input file.

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- 1 5. The method according to claim 1 comprising the step of setting the  
2 START TIME prior to the begin of a functional cycle.
- 1 6. The method according to claim 1 in which the hardware is built according  
2 to silicon-on insulator (SOI) technology.
- 1 7. A computer system having installed program means comprising program  
2 code portions for performing the steps:  
3 (a) carrying out a first DC-simulation run at the begin of a functional  
4 cycle,  
5 (b) carrying out a second DC-simulation run at the end of said cycle,  
6 (c) comparing simulated values from both runs at respective circuit  
7 nodes, and  
8 (d) storing mismatch information about static error afflicted nodes at  
9 which the calculated values differ by more than a predetermined  
10 first threshold value.
- 1 8. The computer system according to claim 7 further comprising program  
2 code portions for performing the steps:  
3 (e) putting out said mismatch information for a manual correction,  
4 (f) carrying out a transient analysis covering the same functional cycle  
5 after correction,  
6 (g) comparing calculated values from said analysis with calculated  
7 values from said first or second DC simulation run at respective  
8 circuit nodes, and  
9 (h) storing mismatch information about dynamic error afflicted nodes at  
10 which the calculated values differ by more than a predetermined  
11 second threshold value.

1 9. A hardware testing computer system having installed program means  
2 comprising program code portions for performing the steps:

- 3 (a) carrying out a first DC-simulation run at the begin of a functional  
4 cycle,  
5 (b) carrying out a second DC-simulation run at the end of said cycle,  
6 (c) comparing simulated values from both runs at respective circuit  
7 nodes, and  
8 (d) storing mismatch information about static error afflicted nodes at  
9 which the calculated values differ by more than a predetermined  
10 first threshold value.

1 10. The computer system according to claim 9 further comprising program  
2 code portions for performing the steps:

- 3 (e) putting out said mismatch information for a manual correction,  
4 (f) carrying out a transient analysis covering the same functional cycle  
5 after correction,  
6 (g) comparing calculated values from said analysis with calculated  
7 values from said first or second DC simulation run at respective  
8 circuit nodes, and  
9 (h) storing mismatch information about dynamic error afflicted nodes at  
10 which the calculated values differ by more than a predetermined  
11 second threshold value.

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FOOTNOTES

1 11. Computer program comprising code portions adapted for performing the  
2 steps below when said program is loaded into a computer system:  
3 (a) carrying out a first DC-simulation run at the begin of a functional  
4 cycle,  
5 (b) carrying out a second DC-simulation run at the end of said cycle,  
6 (c) comparing simulated values from both runs at respective circuit  
7 nodes, and  
8 (d) storing mismatch information about static error afflicted nodes at  
9 which the calculated values differ by more than a predetermined  
10 first threshold value.

1 12. The computer program according to claim 11 further comprising program  
2 code portions for performing the steps:  
3 (e) putting out said mismatch information for a manual correction,  
4 (f) carrying out a transient analysis covering the same functional cycle  
5 after correction,  
6 (g) comparing calculated values from said analysis with calculated  
7 values from said first or second DC simulation run at respective  
8 circuit nodes, and  
9 (h) storing mismatch information about dynamic error afflicted nodes at  
10 which the calculated values differ by more than a predetermined  
11 second threshold value.

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1 13. Computer program product stored on a computer usable medium  
2 comprising computer readable program for causing a computer to perform  
3 the method comprising:

4 (a) carrying out a first DC-simulation run at the begin of a functional  
5 cycle,

6 (b) carrying out a second DC-simulation run at the end of said cycle,

7 (c) comparing simulated values from both runs at respective circuit  
8 nodes, and

9 (d) storing mismatch information about static error afflicted nodes at  
10 which the calculated values differ by more than a predetermined  
11 first threshold value.

1 14. The computer program product according to claim 13 wherein said  
2 method further comprises performing the steps:

3 (e) putting out said mismatch information for a manual correction,

4 (f) carrying out a transient analysis covering the same functional cycle  
5 after correction,

6 (g) comparing calculated values from said analysis with calculated  
7 values from said first or second DC simulation run at respective  
8 circuit nodes, and

9 (h) storing mismatch information about dynamic error afflicted nodes at  
10 which the calculated values differ by more than a predetermined  
11 second threshold value.